Sayan Ghosh

VLSI Design Trainee (ECE Fresher)

sayan.ghosh@example.com +91 90XXX XXX66 Durgapur, West Bengal
linkedin.com/in/sayan-ghosh-example

Personal statement

B.Tech Electronics and Communication Engineering graduate (2026, 8.3 CGPA) focused on digital design and verification. Built an FPGA-based UART and a pipelined MAC unit in Verilog, completed a two-month embedded systems internship, and is looking for a VLSI design or verification trainee role.

Education

B.Tech in Electronics and Communication Engineering · Damodar Valley Institute of Technology, Durgapur, West Bengal 2022 – 2026
Grade: 8.3 CGPA

Class XII (WBCHSE) in Science · Durgapur Model High School, Durgapur, West Bengal 2020 – 2022
Grade: 87%

Class X (WBBSE) in Secondary School · Durgapur Model High School, Durgapur, West Bengal 2019 – 2020
Grade: 90%

Projects

UART Transceiver on FPGA · Final-year project (team of 2) Aug 2025 – Mar 2026

Verilog RTL design synthesised on a Xilinx Artix-7 board.

- Designed the transmitter, receiver and baud-rate generator in Verilog and verified them with a self-checking testbench covering 18 scenarios.
- Achieved error-free transfer at 115200 baud with timing closure at 100 MHz in Vivado.

8-bit Pipelined MAC Unit · Mini project Jan 2025 – Apr 2025

Digital design study comparing array and Booth multipliers.

- Reduced critical path delay by 22% with a 3-stage pipeline, measured from post-synthesis timing reports.

Skills

Verilog · SystemVerilog basics · Xilinx Vivado · FPGA prototyping · Embedded C · STM32 and Arduino · MATLAB · Oscilloscope and logic analyser

Work experience

Embedded Systems Intern · Rupnarayan Embedded Systems Pvt Ltd, Kolkata, West Bengal Jun 2025 – Jul 2025

- Wrote embedded C drivers for an I2C temperature sensor and SPI flash on an STM32 board for an energy-monitoring product.
- Tested 25 prototype PCBs with an oscilloscope and logic analyser and logged faults for the hardware team.
- Reduced sensor read latency by 30% by moving from polling to interrupt-driven I2C.

Certifications

NPTEL: Digital Circuits · NPTEL Nov 2024

NPTEL: Hardware Modeling using Verilog · NPTEL Apr 2025

Core skills

- Digital logic design
- Static timing basics
- Hardware debugging
- Technical documentation
- Team collaboration

Languages

English · Professional · Bengali · Native · Hindi · Fluent

MakePerfectResume · Free